Control of Active Power Exchange With Auxiliary Power Loop in a Single-Phase Cascaded Multilevel Converter-Based Energy Storage System

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***Abstract*—Cascaded multilevel converter (CMC)-based energy storage system, which consists of cascaded H-bridge converters and energy storage components, is a promising option to compensate fluctuating electric power of renewable energy. This paper proposes a novel single-phase CMC-based battery storage system, which includes an *LC* branch. The cascaded converter cells and the *LC* branch form an auxiliary power loop, which could realize active power exchange between different cells with the proposed dual-frequency phase-shifted carrier pulse width modulation (DF-PSC PWM). The principle and effectiveness of DF-PSC PWM and the power transfer mechanism are analyzed. Meanwhile, the design of the tuned filter, output filter, and the state of charge balancing control system is introduced. The operation principle of the power exchange in the proposed energy storage system has been successfully verified by simulation and experimental results.**

***Index Terms*—Auxiliary power loop, cascaded multilevel converter (CMC), energy storage system (ESS), power exchange.**

I. Introduction

THE cascaded multilevel converter (CMC) is a promising solution to obtain high voltage from low-voltage devices. Since switching is between several smaller voltage levels, the CMC has lower *dV*/*dt* than two-level converters. Meanwhile, its modular structure allows the usage of low-cost switching devices with low electromagnetic interference, low total harmonic distribution at low frequency and high fault-tolerance capability [1]. For this reason, CMC has been widely employed in high-power applications such as static synchronous compensator (STATCOM) and motor drivers [2]–[4]. In recent years, its prominent structure makes it suitable for single-phase energy storage applications, which require obtaining high voltage from low-voltage devices, i.e., traction converter in HV with battery [5], [6], regenerative breaking with EDLC [7], [8]. Compared to the traditional transformer-based multipulse converters [9], CMC reduces the voltages of individual energy storage unit. Moreover, high energy efficiency is achieved via its transformerless single-stage circuit structure. The use of CMC in these applications is considered to be a good tradeoff in between complexity and reliability.

Although the number of active switches and control complexity will increase, topology and redundancy allow CMC-based converters to achieve more than one goal within the imposed control system. For example, the dc-link balancing control can be realized without extra circuits. In most CMC applications, the dc-link balancing is fundamental for the safe operation of the system. For CMC-based STATCOMs, adequate methods for maintaining the balance of the capacitor voltages have been employed in the literature [10], [11]. For the CMC-based energy storage system (ESS), the internal impedance and the self-discharge rate are different in each energy storage component, i.e., battery cell or EDLC cell, because of the manufacturing discordances. In a series-connected configuration, the difference of parameter between cells will result in unbalanced voltage/state of charge (SOC). The unbalance of voltage/SOC could reduce the performance of the ESS since some of the cells cannot provide the expected active power while others can. This situation could cause the destruction of the individual energy storage component, and even the failure of the whole system. There have been some balancing circuits for series-connected battery/EDLC packs, which can be classified as passive balancing circuits [12], [13] and active balancing circuits [14]–[18]. The active balancing circuits could effectively equalize the SOC/voltage within series-connected battery/EDLC by transferring energy from cells to cells with dc–dc converters. However, an additional balancing circuit not only increases system complexity but also reduces efficiency. Thus, dc-link balancing control strategies without additional active circuits have been proposed in the literature for a CMC-based system. The voltage balancing methods of single-phase CMC battery energy storage system (BESS) based on staircase modulation have been introduced in [7] and [8]. The main idea is to sort the batteries according to their voltage. By controlling the switch angles, the discharging rate of the battery with highest voltage is higher than others. However, these methods are only effective for staircase modulation. Meanwhile, the voltage balancing speed depends on the load current and cannot be adjusted. The ideas of injecting zero-sequence voltage or negative-sequence current into the three-phase system for dc-link balance are introduced in [19]–[22]. These injected components affect the individual branch powers but keep the total three-phase power transfer unaffected. However, the maximum tolerated voltage variation and semiconductor current rating restrict the injected voltage/current as well as the balancing power [22]. In [23], the

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magnitudes of carrier waves are updated in each ac voltage cycle to change the output voltage of H-bridges. The battery with the highest SOC will discharge at highest rate to diminish the SOC unbalance. However, the differences between carrier wave magnitudes should be limited in certain level to avoid unexpected output voltage levels.

Generally speaking, most existing approaches for dc-link balancing use small shifts of the switching patterns to adjust active power of each energy storage cells [24]–[26]. Since the adjust range is usually limited, the dc-link balancing period is unexpected and the effectiveness depends on the magnitude of the converter current. In addition, design and implementation of multiple balancing control loops are difficult, especially when these are coupled with the fundamental modulators. Considering practical application requires fast balancing during transient disturbances, a balancing control strategy with extra degree of freedoms and independent power control capability is needed.

In [27], a distinct dc-link capacitor voltage control strategy for CMC-based STATCOM is proposed. By injecting orthogonal voltage components, direct control of the balancing current and power are achieved. However, since the fundamental and balancing power flow in the same loop, the output voltage variation of H-bridges is inevitable. Inspired by this idea, a novel active power exchange control strategy is proposed in this paper. By introducing an auxiliary power loop into the CMC and injecting the secondary frequency voltages, a particular H-bridge could generate active power at one frequency and absorb it at another. Thus, the charge/discharge mode of energy storage components in different H-bridges can be controlled individually. With the proposed topology and control strategy, the energy can be directly transferred from one battery to another, from one EDLC cell to another even when the CMC is standby. Since the auxiliary power loop is independent from the fundamental one, the power transfer can be controlled in a relative large range.

This paper is organized as follows: After Section I, a CMC with an auxiliary power loop is proposed in Section II. This converter uses segmented energy storage components as dc source. The dual-frequency phase-shifted carrier pulse width modulation (DF-PSC PWM) used in the proposed system is carefully analyzed. In Section III, the design of tuned filter and output filters is discussed. The power flow control and SOC balancing control strategies are presented to equalize the SOC in a BESS. In Section IV, the proposed system is first simulated in a MATLAB/Simulink simulation platform and then implemented on a 5-kW energy storage test bed. Simulation and experimental results are presented to verify the effectiveness of the proposed system. Finally, conclusion is presented in Section V.

II. System Structure and Power Exchange Principle

A. System Description

The proposed single-phase CMC-based ESS is shown in Fig. 1. The CMC includes *n* series-connected H-bridges and *n* energy storage components. An *LC* branch is paralleled with the cascaded H-bridges, which consists of L_r, C_r, and R_r. The *LC* branch is tuned at resonant frequency f_n. In CMC-based ESS, assignment of *n* is a tradeoff among cost, power quality, and control complexity. At certain voltage level, larger cascaded number may help to reduce the dc voltage of the energy storage devices and increase the equivalent switching frequency. With lower dc voltage, the voltage equalization inside an energy device, i.e., a battery cells string or EDLC cells string, is easier to achieve. With higher equivalent switching frequency, the power quality and power compensation capability can be improved. On the other hand, larger cascaded number increases control difficulty, device count, and total cost. The optimal design of cascaded number and dc voltage is beyond the scope of this paper.

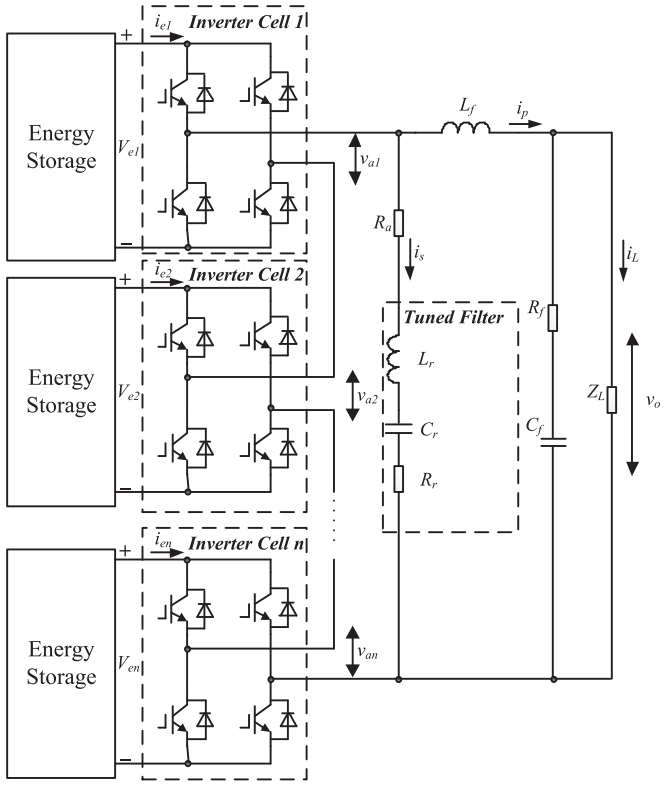

Fig. 1. Topology of proposed CMC with auxiliary power loop.

The active power exchange between energy storage components is based on the orthogonal power flow theory [28]. Considering nonsinusoidal voltage *v*(*t*) and current *i*(*t*) which contains sinusoidal components at different frequency

$$v(t) = V_0 + \sum_{n=1}^{\infty} \sqrt{2} V_n \cos(n\omega t + \theta_n) \tag{1}$$

$$i(t) = I_0 + \sum_{n=1}^{\infty} \sqrt{2} I_n \cos(n\omega t + \varphi_n). \tag{2}$$

If the active power resulting from the *v*(*t*) and *i*(*t*) is considered to be the average value of the product of their instantaneous values over a certain small period of time, the average active power *P* in one short period can be expressed by

$$P = V_0 I_0 + \sum_{n=1}^{\infty} V_n I_n \cos(\theta_n - \varphi_n). \tag{3}$$

According to (3), if the PWM waveforms for the H-bridges contain an auxiliary frequency component f_a, which is higher

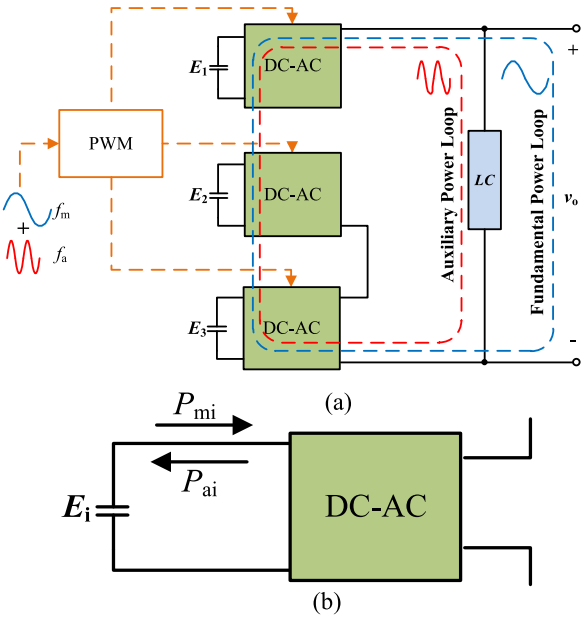

Fig. 2. Power flow. (a) Fundamental and auxiliary power loop. (b) Power flow of single cell.

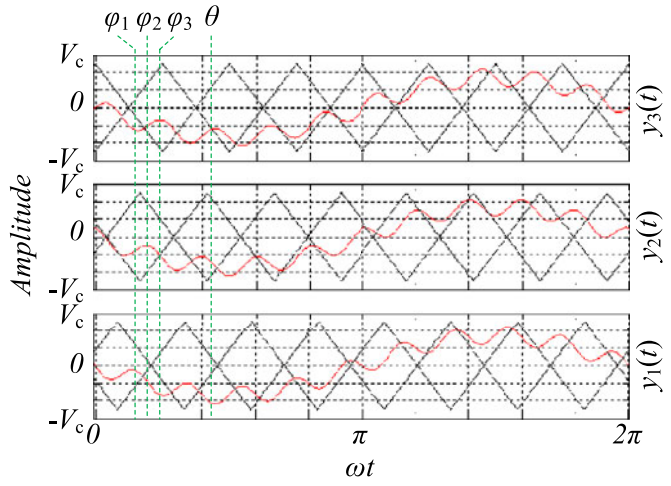

Fig. 3. Reference and carriers of seven-level DF-PSC PWM operation.

than the fundamental frequency f_m, one H-bridge can provide active power at f_m and absorb at f_a. Fig. 2(a) illustrates the power flows of the proposed ESS. E_1–E_3 can be battery, EDLC or other energy storage components. The modulation wave of PWM control contains two frequencies: f_m and f_a. f_a is equal to the resonant frequency of the series *LC* branch f_n. With the frequency-selecting feature of the series *LC* branch, the power produced by voltage and current at f_a, which is defined as auxiliary power, will be kept in an auxiliary power loop made up by H-bridges 1–3 and the *LC* branch. Meanwhile, the power produced by the voltage and current at f_m, which is defined as the fundamental power, flows to the load. The auxiliary frequency f_a has to be higher than the fundamental frequency f_m or it cannot be eliminated in the output voltage. Higher f_a will also help to design the output filer and reduce the sizing of the tuned filter. However, considering the possible shift of the resonant inductance, high f_a will affect the accuracy of power control in the auxiliary power loop. Meanwhile, since PWM control is used in generating the dual-frequency voltage, the switching frequency of the converter also restricts the upper level of f_a. In the simulation and experiment of this paper, the fundamental frequency is 50 Hz, the carrier frequency f_c is 5000 Hz, and the f_a to f_m factor is designed to be 10. Thus, f_a is ten times of f_m and f_c is ten times of f_a. With this configuration, f_a can be easily filtered from the output filter and the quality of the auxiliary power can be guaranteed.

As shown in Fig. 2(b), in the *i*th H-bridge, the auxiliary power $P_{\rm mi}$, and fundamental power $P_{\rm ai}$ can be controlled independently. Thus, the charge/discharge states of the energy storage components can be different, depending on the direction and amount of $P_{\rm mi}$ and $P_{\rm ai}$. When $P_{\rm ei} = P_{\rm mi} + P_{\rm ai}$ and $P_{\rm ei} > 0$, E_i is in discharge state, the active power provided by E_i is absorbed by the load or other energy storage components. When $P_{\rm ei} < 0$, E_i is in charge state and its energy reservation can be improved. When $P_{\rm ei} = 0$, E_i is in standby state.

In this paper, the configuration is applied to a BESS-based on CMC. To simplify the analysis, the number of H-bridges is selected to be three. The dc voltage of each inverter cell is selected to be 24 V.

B. Principle of DF-PSC PWM

The main advantage of the proposed cascaded ESS is that the power exchange control between energy storage components and the active power control of the ESS are decoupled with each other. The DF-PSC PWM modulation method is adopted to generate gate signals of switches in H-bridges.

Like traditional phase-shifted carrier PWM technique, *N*-level operation of DF-PSC consists of *N*–1 symmetrical triangular carriers, but in DF-PSC, the reference waveforms are hybrid modulations $y_i(t)(i = 1, \ldots, N-1)$ combining two sine waves at f_m and f_a. In each $y_i(t)$, the sine waves at f_m are of the same phase, but there are phase differences between the sine waves at f_a, which determine the power exchange between H-bridges. For configuration in Fig. 1, there is

$$\begin{aligned} y_i(t) &= V_{\rm mmi}\sin(\omega_m t + \theta) + V_{\rm mai}\sin(\omega_a t + \varphi_i), \\ i &= 1, 2, 3 \end{aligned} \tag{4}$$

where $\omega_m = 2\pi f_m$ and $\omega_a = 2\pi f_a$, $V_{\rm mmi}$ and $V_{\rm mai}$ are peak values of sine waves at f_m and f_a, respectively, and φ_i represents phase angle of the high frequency part. Fig. 3 shows the carriers and the hybrid modulation reference waveform for a seven-level PWM using DF-PSC.

Since two different frequency components are combined in DF-PSC, the intersections of reference and carrier waveform are different from the traditional PWM. Thus, the existing mathematic conclusions of PWM voltage waveforms cannot be used to analyze the DF-PSC output voltage. In this section, the mathematical model of DF-PSC is derived and voltage components at different frequencies are achieved.

The dc voltage of each energy storage component is set to V_c. The fundamental modulation depth is defined as $M_i = V_{\mathrm{mmi}}/V_c \leq 1$. The auxiliary modulation depth is defined as $N_i = V_{\mathrm{mai}}/V_c \leq 1$. The carrier wave ratio of auxiliary frequency $F_a = f_c/f_a \gg 1$. f_c represents the frequency of symmetrical triangular carrier. The dc voltage of each energy storage component is set to V_c. For H-bridge *i*, the DF-PSC PWM voltage $\nu_{\mathrm{ai}}(x,y)$ is about the following periodic time variables:

$$x(t) = \omega_c t + \theta_c \tag{5}$$

$$y(t) = \omega_m t + \theta_m, \tag{6}$$

where θ_c and θ_m are initial phase of carrier and reference waveforms. The time-domain expression of $\nu_{\mathrm{ai}}(x,y)$ is

$$\nu_{\mathrm{ai}}(x,y) = \begin{cases} \dfrac{V_c}{2}x \begin{cases} \geq 2(k+1)\pi - \alpha_c - \dfrac{\pi}{2}(1 + M_i \sin y \\ \quad + N \sin qy) \\ < 2k\pi - \alpha_c + \dfrac{\pi}{2}(1 + M_i \sin y \\ \quad + N_i \sin qy) \end{cases} \\ -\dfrac{V_c}{2}x \begin{cases} \geq 2k\pi - \alpha_c - \dfrac{\pi}{2}(1 + M_i \sin y \\ \quad + N_i \sin qy) \\ < 2(k+1)\pi - \alpha_c - \dfrac{\pi}{2}(1 + M_i \sin y \\ \quad + N_i \sin qy). \end{cases} \end{cases} \tag{7}$$

Based on the double Fourier series theory, (7) could be expanded as

$$\begin{aligned} \nu_{\mathrm{ai}}(x,y) = {} & \frac{A_{00}}{2} + \sum_{n=1}^{\infty}(A_{0n}\cos nx + B_{0n}\sin ny) \\ & + \sum_{m=1}^{\infty}(A_{m0}\cos mx + B_{m0}\sin my) \\ & + \sum_{m=1}^{\infty}\sum_{n=\pm 1}^{\pm\infty}[A_{\mathrm{mn}}\cos(mx+ny) \\ & + B_{\mathrm{mn}}\sin(mx+ny)]. \end{aligned} \tag{8}$$

The coefficients of each term in (8) can be determined with integral expression

$$A_{\mathrm{mn}} + jB_{\mathrm{mn}} = \frac{2}{(2\pi)^2}\int_{-\pi}^{\pi}\int_{-\pi}^{\pi}\nu_i(x,y)e^{j(\mathrm{mx+ny})}dxdy. \tag{9}$$

By substituting (7) into (9), there is

$$\begin{aligned} A_{\mathrm{mn}} + jB_{\mathrm{mn}} = {} & -\frac{jV_c}{m\pi^2}\int_{-\pi}^{\pi}\Big[e^{j\left[\frac{m\pi}{2}+\frac{m\pi}{2}(M_i\sin y + N_i\sin qy)\right]} \\ & - e^{-j\left[\frac{m\pi}{2}+\frac{m\pi}{2}(M_i\sin y + N_i\sin qy)\right]}\Big]e^{-jm\theta_c} \\ & \times e^{\mathrm{jny}}dy \\ = {} & \frac{V_c}{m\pi^2}\int_{-\pi}^{\pi}2\sin\Big[\frac{m\pi}{2} + \frac{m\pi}{2}(M_i\sin y \\ & + N_i\sin qy)\Big]e^{-jm\theta_c}e^{\mathrm{jny}}dy. \end{aligned} \tag{10}$$

By solving (10), we have

1) DC component

When $m = 0$ and $n = 0$, $A_{00} = 0$.

2) Fundamental and baseband harmonic components

When $m = 0$ and $\neq 0$, (10) can be derived as

$$\begin{aligned} A_{0n} + jB_{0n} = {} & \frac{V_c}{\pi^2}\int_{-\pi}^{\pi}\pi\left[1 + [M_i\sin y + N_i\sin qy]\right]e^{\mathrm{jny}}dy \\ = {} & \frac{V_c}{\pi^2}\int_{-\pi}^{\pi}\pi j\left(M_i\sin y\sin ny + N_i\sin qy\sin ny\right)dy. \end{aligned} \tag{11}$$

From (11), we can obtain following equations

$$A_{01} + jB_{01} = jM_iV_c, \quad n = 1 \tag{12}$$

$$A_{0q} + jB_{0q} = jN_iV_c, \quad n = q \tag{13}$$

$$A_{0n} + jB_{0n} = 0, \quad n \neq 1 \quad \text{and} \quad n \neq q. \tag{14}$$

When (12) and (13) are combined and the carrier harmonic components and sidebands harmonic components are neglected, the output voltages of one H-bridge is

$$\nu_i(t) = M_iV_c\sin(\omega_m t + \theta) + N_iV_c\sin(\omega_a t + \varphi_i). \tag{15}$$

Equation (15) reveals a simple but important conclusion about DF-PCS: The amplitudes of the two output voltage components at different frequencies are independent. With (4) and (15), the superimposed effectiveness of DF-PSC PWM is proved mathematically. That means the modulation depths of two voltage components can be determined, respectively, and the controls of fundamental power loop and auxiliary power loop are decoupled with each other.

C. Power Exchange Control Methods Analysis

In Fig. 2, the fundamental frequency current flow in three H-bridges is the same because of the series configuration. If M_i $(i = 1, 2, 3)$ are identical, the active power produced by current and voltage at fundamental frequency of the CMC is equal to P_m, which is delivered to the load. Based on the orthogonal power flow theory, we can analyze the power produced by current and voltage at auxiliary frequency independently. In power exchange application, we assume that the energy in E_1 need to be transferred to E_3. Thus, in auxiliary power loop, E_1 needs be in "discharging" state, E_3 in "charging" state, and E_2 in "standby" state, i.e., there is no active power exchange between E_2 and the other two components. The quotation marks imply that these operation states are defined in auxiliary power loop. E_1–E_3 are actually all in discharging state in the fundamental power loop.

A phase-shifted power exchange control method is proposed to manipulate the operation states of E_1–E_3 in auxiliary power loop. In order to simplify the analysis of the converter, the following assumptions are made:

1) the dc voltages of all energy storage components are constant V_c;
2) current flow at auxiliary frequency is kept in the auxiliary power loop;

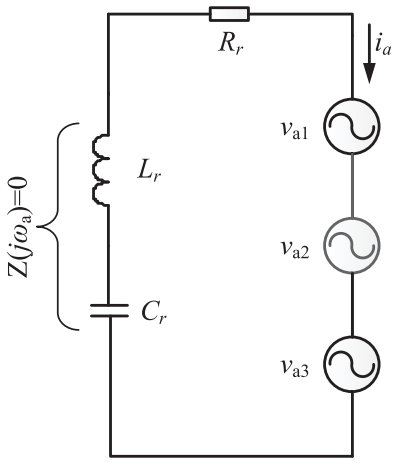

Fig. 4. Equivalent circuit of auxiliary power loop.

3) the equivalent impedance of the series *LC* branch at f_a is pure resistance ($Z(j\omega_a) = R_r$);
4) all switches, diodes, inductor, and capacitor are ideal components.

With the aforementioned assumptions, the simplified equivalent circuit is shown in Fig. 4. i_a is the auxiliary frequency current flowing in the loop. $\nu_{a1} - \nu_{a3}$ are the equivalent auxiliary frequency voltage sources representing three H-bridges. We have

$$\nu_{\rm ai}(t) = V_{\rm ai}\sin(\omega_a t + \varphi_i), \quad i = 1, 2, 3. \tag{16}$$

where $V_{\rm ai} = N_i V_c$.

To illustrate the phase-shifted power exchange principles, the vector diagram of current and voltages inside the auxiliary power loop is depicted in Fig. 5. $\dot{V}_{a1} - \dot{V}_{a3}$ and $\dot{I}_a$ are vectors of $\nu_{a1} - \nu_{a3}$ and i_a, respectively. $\dot{V}_a$ is the summation of $\dot{V}_{a1} - \dot{V}_{a3}$ and $\dot{V}_{a12}$ of $\dot{V}_{a1}$ and $\dot{V}_{a2}$. Since the equivalent impedance of the loop is pure resistance, $\dot{V}_a$ is in phase with $\dot{I}_a$. To clearly describe the power exchange, $\dot{V}_a$ and $\dot{I}_a$ lead 90° to *x*-axis in Fig. 5.

In this control method, N_i is constant and the phase differences are shifted to change the power exchange. $\dot{V}_{a1\_p}$, $\dot{V}_{a2\_p}$, $\dot{V}_{a1\_q}$, and $\dot{V}_{a2\_q}$ are active and reactive components of $\dot{V}_{a1}$ and $\dot{V}_{a2}$. In previous assumption, E_3 is in standby state and E_1 provides active power to E_2. Thus, $\dot{V}_{a3}$ should lead 90° to $\dot{I}_a$, $\dot{V}_{a1\_p}$ is in phase with $\dot{I}_a$ and $\dot{V}_{a2\_p}$ is opposite in phase with $\dot{I}_a$.

The active power contributed by E_1 contains two components: the power absorbed by E_2 and the power consumed by R_r. There is

$$\dot{V}_{a2\_p}\dot{I}_a + \dot{V}_a\dot{I}_a = \dot{V}_{a1\_p}\dot{I}_a. \tag{17}$$

From (17) and Fig. 5(a), it is obvious that the active power exchange between E_1 and E_2 is

$$P_e = V_{a2}\sin\varphi_2 I_a = V_{a2}\sin\varphi_2\frac{V_a}{R_r}. \tag{18}$$

From (18), P_e can be adjusted by V_{a2}, V_a or φ_2. V_a is coupled with $\dot{V}_{a1}$ and $\dot{V}_{a2}$. To reduce the control complexity, we assume

$$V_{a1} = V_{a2} = V_{\rm ah} = N_h V_c. \tag{19}$$

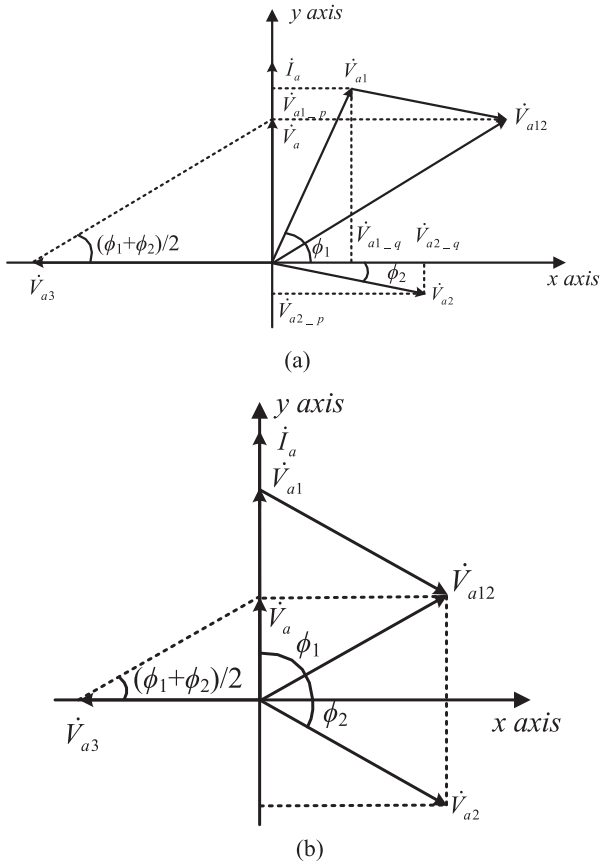

Fig. 5. Vector diagram of phase-shifted control. (a) general phase-shifted control. (b) MPEP of phase-shifted control.

By analyzing the vector diagram, we have

$$V_{a12} = 2V_{\rm ah}\cos\frac{\varphi_1 - \varphi_2}{2} \tag{20}$$

$$V_a = V_{\rm ah}(\sin\varphi_1 + \sin\varphi_2) \tag{21}$$

$$I_a = \frac{V_a}{R_r} = \frac{V_{\rm ah}(\sin\varphi_1 + \sin\varphi_2)}{R_r}. \tag{22}$$

The existence of (17)–(19) depends on the amplitude of the E_3. There is

$$V_{a3} = V_{\rm ah}(\cos\varphi_1 + \cos\varphi_2). \tag{23}$$

From (17) to (19), we have

$$P_e = \frac{V_{\rm ah}^2(\sin\varphi_1 + \sin\varphi_2)\sin\varphi_2}{R_r} \tag{24}$$

$$P_{\rm loss} = \frac{V_{\rm ah}^2(\sin\varphi_1 + \sin\varphi_2)^2}{R_r} \tag{25}$$

where $P_{\rm loss}$ is the power loss of R_r.

From Fig. 5(a), it can be seen that the ranges of shifted phase are $\varphi_1 \in [0, \pi/2]$ and $\varphi_2 \in [-\pi/2, 0]$. The partial differential equation derived from (24) is

$$\begin{cases} f_{\varphi_1} = \cos\varphi_1\sin\varphi_2 = 0 \\ f_{\varphi_2} = \cos\varphi_2(\sin\varphi_1 + 2\sin\varphi_2) = 0. \end{cases} \tag{26}$$

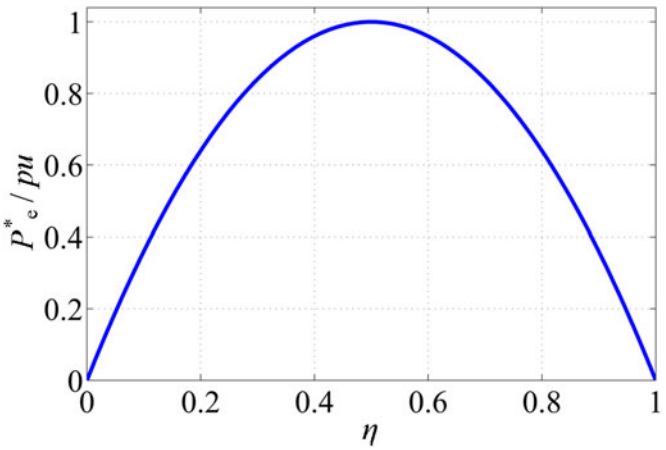

Fig. 6. Efficiency versus power exchange (p.u.).

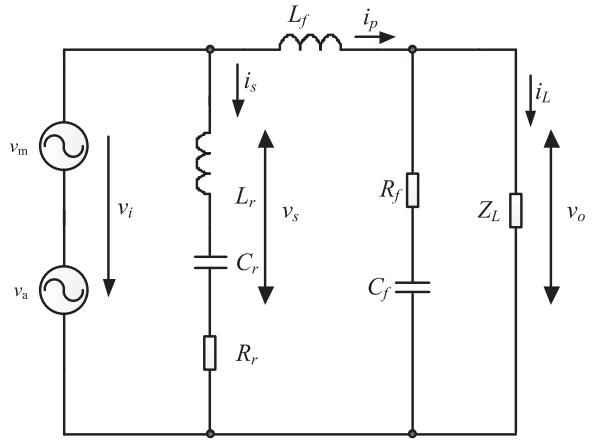

Fig. 7. Equivalent circuit with ac source and filters.

The MPEP of phase-shifted control appears at one of the stagnation points of (26) as shown in Fig. 5(b). When $\varphi_1 = \frac{\pi}{2}$ and $\varphi_2 = -\frac{\pi}{6}$, the maximum power exchange of phase-shifted control is

$$P'_{e\_\mathrm{mpep}} = P'_{\mathrm{loss\_mpep}} = -\frac{V^2_{\mathrm{ah}}}{4R_r}. \tag{27}$$

From vector diagram, we can find that the power exchange efficiency can be improved by reducing the difference between $\dot{V}_{a1\_p}$ and $\dot{V}_{a2\_p}$. Consequently, the power exchange will decrease since auxiliary power loop current i_a is inversely proportional to $\dot{V}_{a1_p} - \dot{V}_{a2_p}$. In Fig. 6, the vertical axis is the per-unit value of exchanged power P^*_e and the horizontal axis is the efficiency η. It can be seen that when efficiency approaches 100%, the power exchange approaches 0.

III. Circuit Parameter and Control System Design

A. Output Filter Design

The design of tuned filter and output filter is discussed in this section. The equivalent circuit with ac source and filters is shown in Fig. 7. The summations of output voltages at fundamental frequency ($\nu_{m1} - \nu_{m3}$) and auxiliary frequency ($\nu_{a1} - \nu_{a3}$) are simplified to equivalent ac sources ν_m and ν_a. There is $\nu_s = \nu_m + \nu_a$. The tuned filter consists of L_r, C_r, and R_r. Its objective is to generate a low-impedance path for the auxiliary frequency current i_a. The output filter consists of L_f, C_f, and R_f. Its objective is to guarantee the output power quality of the inverter. The filter resistor R_f is designed to result in an overdamped circuit. R_f can be set equal to the characteristic impedance of the cable to absorb the reflected energy [29]. There is

$$R_f \geq \sqrt{\frac{4L_f}{C_f}}. \tag{28}$$

Considering the harmonic cancellation in a cascaded single-phase converter, ν_s could be expressed as

$$\begin{aligned}\nu_s(t) &= MnV_c \sin(\omega_m t + \theta) + NnV_c \sin(\omega_a t + \varphi_i) + \frac{2V_c}{\pi} \\ &\times \sum_{m=1}^{\infty} \sum_{\substack{k=-\infty \\ k\neq 0}}^{\infty} \frac{1}{m} \{\cos([nm + k + 1]\pi)[J_{2k-1} \\ &\times (nmM\pi)\cos(2nm\omega_c t + (2k-1)\omega_m t) + J_{2k-1}) \\ &\times (nmN\pi\cos(2nm\omega_c t + (2k-1)\omega_a t)]\}. \end{aligned} \tag{29}$$

From (29), it could be concluded that the only harmonics components in ν_s are sideband harmonic components centered around 2*n*th carrier multiple. For three cascaded H-bridges, the sidebands harmonic components concentrate around $6mf_c (m = 1, \ldots, \infty)$.

The auxiliary frequency component and the sidebands harmonic components are unwanted in ν_o. Thus, the target of output filter is to eliminate the second and third parts in (29). Since f_c is usually ten times f_a, the objective of the filter is mainly to reduce the amplitude of auxiliary frequency voltage in ν_o. The ν_s to ν_o transfer function is

$$\nu_o(s) = H\nu_s(s) = \frac{1 + sR_fC_f}{1 + s^2L_fC_f + sR_fC_f}\nu_s(s). \tag{30}$$

The cutoff frequency of the output filter should be smaller than the auxiliary frequency f_a and larger than the fundamental frequency f_m. Since the carrier frequency is several ten times of f_m, following equation is used to determine the cutoff frequency f_{ct}

$$\frac{f_c}{30} \leq f_{\mathrm{ct}} \leq \frac{f_a}{2}. \tag{31}$$

The lower limit of f_{ct} is reduced to match the relative low upper limit. With $f_a = 500$ Hz and $f_c = 5000$ Hz, $f_{\mathrm{ct}} = 180$ Hz is selected to design the output filter. The selected attenuation is 3 dB at the cutoff frequency, where the effective attenuation in decibels issdeqn

$$A = 20\log\left|\frac{1}{H}\right|. \tag{32}$$

With (30)–(32), there is

$$3 = 20\log\frac{1 + L_fC_f\omega^2_{\mathrm{ct}}}{\sqrt{1 + 4L_fC_f\omega^2_{\mathrm{ct}}}}, \tag{33}$$

where $\omega_{\rm ct} = 2\pi f_{\rm ct}$. Solving (28) and (33) with an attenuation of 3 dB at the cutoff frequency 180 Hz yields $L_f = 3.2$ mH, $C_f = 124.85$ μF and $R_f = 10.12$ Ω. The simulation result of the designed output filter will be shown in Section IV.

B. Tuned Filter Design

The tuned filter has three passive components: resonant inductor L_r, resonant capacitor C_r, and resonant resistor R_r. The ideal relation between resonant capacitance and inductance in the tuned filter is

$$\omega_a L_r = \frac{1}{\omega_a C_r} \tag{34}$$

where $\omega_a = 2\pi f_a$.

Ideally, to create a low-impedance path for auxiliary frequency current, L_r and C_r can be designed arbitrarily according to (34). However, two factors will affect the selection of L_r and C_r: the impedance of *LC* branch at fundamental frequency and the possible shift of resonant parameter.

With (34), the impedance of the tuned filter can be calculated as

$$Z_r = R_r + jL_r\left(\omega - \frac{\omega_a^2}{\omega}\right). \tag{35}$$

From (35), it is obvious that the impedance of the tuned filter at fundamental frequency and its harmonic components increase with L_r. Thus, the power loss caused by Z_r at f_m is

$$P_{\rm loss\_m} = \frac{9M_h^2V_c^2}{2\sqrt{\left[R_r^2 + (\omega_m' L_r)^2\right]}}\cos\varphi_m, \tag{36}$$

where $\omega_m' = \omega_m - \frac{\omega_a^2}{\omega_m}$, $\varphi_m = \arctan\frac{\omega_m' L_r}{R_r}$, $M_{\rm h}$ is the common maximum fundamental modulation depth of three H-bridges.

If only considering the reduction of $P_{{\rm loss}_m}$, large L_r should be selected. However, the possible shift of resonant parameters should be considered. If the resonant inductance shifts to $L = L_r + \Delta L$, the actual impedance of *LC* branch at f_a is

$$Z_{rr} = R_r + j\omega_a\Delta L = \sqrt{R_r^2 + (\omega_a\Delta L)^2}\angle\Delta\varphi, \tag{37}$$

where $\Delta\varphi = \arctan\dfrac{\omega_a\Delta L}{R_r}$.

With the vectors of voltages in Fig. 5(a) and (37), the auxiliary current can be calculated

$$\dot{I}_a = \frac{\dot{V}_a}{Z_{rr}} = \frac{V_{\rm ah}\left(\sin\varphi_1 + \sin\varphi_2\right)}{\sqrt{R_r^2 + (\omega_a\Delta L)^2}}\angle\left(\frac{\pi}{2} - \Delta\varphi\right). \tag{38}$$

From (38), it can be seen that the shift of resonant inductance will cause the deviation of auxiliary current from $\frac{\pi}{2}$ and the decrease of its magnitude. Thus, the exchanged power of E_1–E_3 will deviate from the theory values. For example, the output active power of E_3 will change from 0 to

$$P_3 = \frac{V_{\rm ah}^2\left(\sin\varphi_1 + \sin\varphi_2\right)\left(\cos\varphi_1 + \cos\varphi_2\right)}{\sqrt{R_r^2 + (\omega_a\Delta L)^2}}\cos\left(\frac{\pi}{2} + \Delta\varphi\right). \tag{39}$$

TABLE I
LC BRANCH DESIGN PARAMETER

Item	Symbol	Value
Fundamental modulation depth	M_h	0.7
Auxiliary modulation depth	N_h	0.3
DC voltage of energy storage components	V_c	24 V
Maximum auxiliary power	$P_{e\max}$	100 W
Allowable fundamental power loss	$P_{\rm loss\_m}$	1 W
Tolerance of resonant inductance	$\Delta L_r/L_r$	$\leq\pm2\%$
Maximum allowable $\Delta\varphi$	$\Delta\varphi$	$\leq 5^\circ$
Auxiliary frequency	f_a	500 Hz
Fundamental frequency	f_m	50 Hz

With tolerance of resonant inductance, i.e., $\pm2\%$, $\Delta\varphi$ can be minimized by reducing L_r or increasing R_r. As shown in (24) and (25), R_r determines the exchanged power, the SOC balancing speed, and the power loss. Increasing R_r may diminish the performance and efficiency of the SOC balancing control. Meanwhile, reducing L_r may include fundamental current into the auxiliary power loop. The power produced by current and voltage at fundamental frequency will also affects the efficiency of the system. Thus, the design of the resonant parameters L_r and R_r is a tradeoff between power control accuracy and power loss.

Based on above analysis, L_r and R_r can be designed with following procedure:

1) based on (27), determine R_r with dc voltage V_c, auxiliary modulation depth N_h, and preferred maximum auxiliary power $P_{e\max}$;
2) based on (36), determine the lower threshold of resonant inductance $L_{r_{\rm low}}$ with allowable $P_{\rm loss\_m}$;
3) based on (37), determine the upper threshold of resonant inductance $L_{r_{\rm high}}$ with tolerance of L_r, allowable $\Delta\varphi$ and R_r;
4) optimal selection of L_r can be searched between $L_{r_{\rm low}}$ and $L_{r_{\rm high}}$ by comprehensively considering loss, cost, and volume. With selected L_r, C_r can be obtained with (34).

To illustrate the design procedure, the tuned filter is designed with the parameters in Table I.

With parameters in Table I, the upper and lower thresholds of L_r are 1.5 and 1.6 mH, respectively. The resistance of the *LC* branch $R_r = 0.18$ Ω. If L_r is selected to be 1.55 mH, the resonant capacitance will be $C_r = 65.369$ μF. At this condition, the maximum active power E_3 absorbs is about 9.6 W and $P_{{\rm loss}_m}$ is below 1 W, which is within the acceptable range.

C. SOC Balancing Control

In CMC with integrated energy storage, unbalanced SOC values have a negative effect on the normal operation of the system. Although the proposed power exchange control method based on DF-PSC PWM could be used in various fields, we choose SOC balancing control as an example to illustrate the decoupled energy control loops. However, in this paper, we do not intend to explore such SOC balancing issues as optimized algorithm and balancing speed comparison. The SOC balancing control is used to verify the proposed power exchange theories.

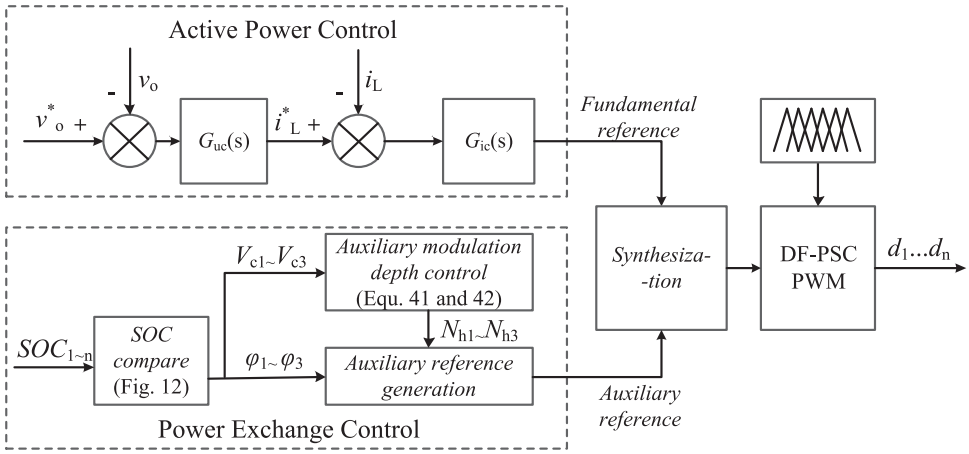

Fig. 8. Control block of battery SOC balancing control strategy.

Fig. 8 shows the simple control block diagram of an n cells single-phase inverter with segmented batteries as dc source. The whole control is divided into two separate subcontrols: the active power control of the inverter and the power exchange control between cells.

Since the power exchange control and output voltage control are decoupled with each other, existed control methods for single-phase CMC inverter can be employed to obtain the reference waveform at f_m. The active power control method selected in this paper is voltage–current double-loop control, which is the classic control method for a single-phase inverter. In the active power control block, the output voltage ν_o is compared with its reference ν_o^* and the error signal is processed by the outer voltage loop compensator $G_{\rm uc}(s)$ to obtain the reference for inductor current i_L^*. i_L^* is compared with inductor current i_L and the error signal is processed by the inner current loop compensator $G_{\rm ic}(s)$ to obtain fundamental reference signal. $G_{\rm uc}(s)$ is a PI controller and $G_{\rm ic}(s)$ is a PID controller.

The fundamental reference signal will be synthetized with the auxiliary reference signal, which is generated by the power exchange control block, to obtain the modulation signal for the proposed DF-PSC PWM control. The control signals of the active switches in each H-bridge of the BESS are generated with DF-PSC PWM control and drive circuit.

The auxiliary reference signals for H-bridges are not identical. The three H-bridges are defined as the energy source (ES), energy destination (ED), and balance cell (BC). In these H-bridges, high-frequency references $\nu_{a1} - \nu_{a3}$ are added to fundamental reference for power exchange. For other H-bridges, only fundamental references are used to generate switching signals. First, the SOCs of all batteries are compared to select current ES, ED, and BC. As shown in Fig. 9, in SOC compare block, the batteries with maximum SOC and minimum SOC (E_i and E_j) are selected as the ES and ED. The battery with the closest value to the average SOC of E_i and E_j could be selected as BC. The target of SOC balancing control is to limit the maximum SOC difference between cells to ΔSOC. If the SOC of ES is defined as $\rm SOC_{ES}$, the SOC of ED is defined as $\rm SOC_{ED}$, the control target is $\rm SOC_{ES} - SOC_{ED} > \Delta SOC$. Meanwhile, considering

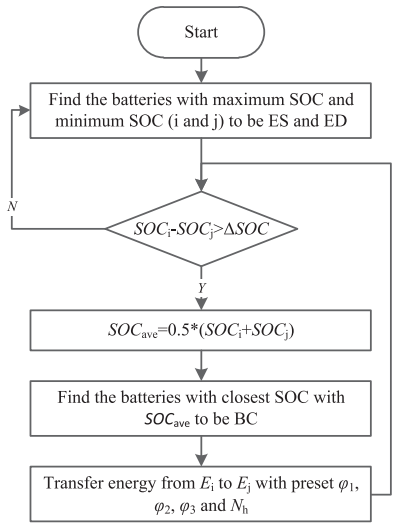

Fig. 9. SOC compare algorithm.

the possible unbalanced dc voltages of the batteries in these H-bridges, the auxiliary modulation depths should be controlled to make the assumption in (19) and (23) exist. The auxiliary modulation depth of ES is preset as N_{h1}. Following equations are used to obtain N_{h2} and N_{h3} for ED and BC cells

$$N_{h2}(s) = N_{h1}\frac{\nu_{c1}}{\nu_{c2}} \tag{40}$$

$$N_{h3}(s) = 2N_{h1}\frac{\nu_{c1}}{\nu_{c3}(\cos\varphi_1 + \cos\varphi_2)} \tag{41}$$

where $\nu_{c1} - \nu_{c3}$ are the dc voltage of batteries in ES, ED, and BC, and φ_1–φ_3 are the preset phase-shifted angles for ES, ED, and BC. Since the power exchange and SOC variation processes are slow, transient disturbances of output voltage and current will not affect the SOC balancing process. Thus, the power exchange control is open loop with preset φ_1–φ_3 and N_{h1}, which are chosen with power loss and SOC balancing speed considerations.

TABLE II
SIMULATION PARAMETERS

Item	Symbol	Value
Rated Voltage	V_c	24 V
Rated Capacity	C_b	5 AH
ESR	R_{esr}	0.1 Ω
Initial SoC	SOC_0	0.6
Carrier frequency	f_c	5000 Hz
Auxiliary frequency	f_a	500 Hz
Fundamental frequency	f_m	50 Hz
Inductance of output filter	L_f	3.2 mH
Capacitance of output filter	C_f	124.85 μF
Resistance of output filter	R_f	10.12 Ω
Inductance of tuned filter	L_r	2 mH
Capacitance of tuned filter	C_r	50 μF
Resistance of tuned filter	R_r	0.1 Ω
Fundamental Modulation Depth	M_h	0.7
Auxiliary Modulation Depth	N_h	0.3
Phase angle of ES	φ_1	$\pi/2$
Phase angle of ED	φ_2	$-\pi/6$
Phase angle of BC	φ_3	π
H-Bridge Number	n	3
Peak Output Voltage	V_{om}	50 V
Load	R_L	50 Ω

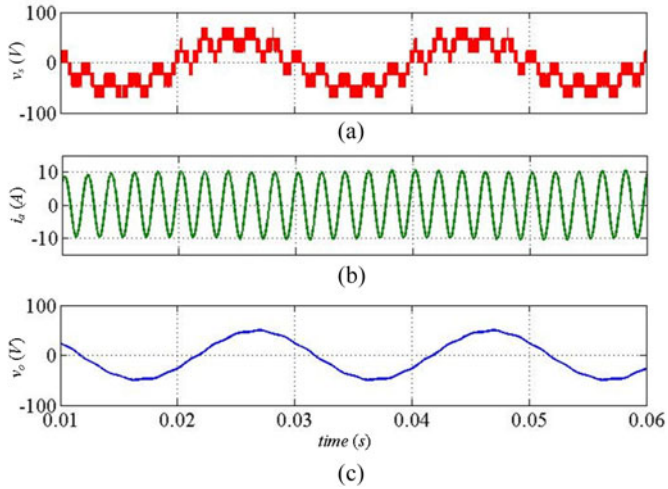

Fig. 10. Three-cells cascaded ESS output waveforms. (a) Output voltage of the cascaded H-bridges. (b) Auxiliary current. (c) System output voltage.

With φ_1–φ_3 and $N_{h1} - N_{h3}$, auxiliary reference signals are generated. When $\varphi_1 = \frac{\pi}{2}$, $\varphi_2 = -\frac{\pi}{6}$, and $\varphi_3 = \pi$, we have the maximum power exchange between ES and ED. The fundamental reference and auxiliary reference are synthesized to generate switching signals with DF-PSC PWM control strategy. With DF-PSC PWM control, the power exchange between ES and ED would reduce their SOC difference. When $\mathrm{SOC_{ES}} - \mathrm{SOC_{ED}} \leq \Delta\mathrm{SOC}$, current power exchange process stops and the control system starts to find the next pair of unbalanced batteries, until the SOC values of all the batteries are balanced.

IV. SIMULATION AND EXPERIMENTAL RESULTS

In order to verify the proposed topologies and theoretical analysis, the model of a BESS with cascaded H-bridges and a tuned filter are simulated with MATLAB/SIMULINK simulation software. The detailed parameters are listed in Table II.

The output waveforms of open-loop simulation with preset parameters are shown in Fig. 10, in which (a) shows the output voltage of the cascaded H-bridges ν_s, (b) shows the auxiliary current in the tuned filter i_o, and (c) shows the system output voltage of the $\nu_o.\nu_s$ is seven-levels step waveform modulated with DF-PSC PWM. Because of the frequency effect of the tuned filter, i_a is 500 Hz sinusoidal current. The system output voltage ν_o is 50 Hz sinusoidal wave since the output filter eliminates the auxiliary frequency component and the sidebands harmonic components in ν_s. The peak output voltage is regulated at 50 V. That proves the effectiveness and independence of active power control.

To verify the relation between the amplitudes of the two output voltage components at different frequencies revealed in (15), the fast Fourier transform (FFT) analysis of ν_s is shown in Fig. 11. The amplified figure on the left indicates that the amplitude of auxiliary frequency (500 Hz) part is about 42.86% of that of the fundamental frequency (50 Hz) part. The proportion is very close to the modulation depth ratio (N/M = 0.3/0.7). Meanwhile, the amplified figure on the right proves the conclusion about the sideband harmonic components in (29). The sidebands harmonic components concentrate around $m \times 6 \times 5$ kHz$(m = 1, \ldots, \infty)$. The rest harmonic components are cancelled by the DF-PSC PWM. In Fig. 11, the sidebands harmonic frequencies are 30, 60, and 90 kHz.

To verify the power exchange mechanism between the inverter cells via auxiliary power loop, the phase lags of the auxiliary frequency references φ_1, φ_2, and φ_3 are set to $-\frac{\pi}{6}$, $\frac{\pi}{2}$, and π. The waveforms of the auxiliary current i_a, the power produced by auxiliary current, and the voltage of the three inverter cells $p_{e1} - p_{e3}$ are shown in Fig. 12. The magnitude of the i_a is 7.2 A, which proves our conclusion about I_a of phase-shifted control in (22). The frequencies of the power produced by auxiliary currents and voltages are twice the frequency of i_a. It is obvious that the average values of p_{e1}, p_{e2}, and p_{e3} are, respectively, positive, negative, and zero. This phenomenon verifies that H-bridge 1 provides power to H-bridge 2 via auxiliary power loop. Meanwhile, H-bridge 3 provides pure inactive power to sustain the power exchange.

To verify the effectiveness of active power exchange in SOC balancing control, different configurations of BESS with the proposed topology were simulated with the control strategy introduced in Fig. 8. First, a BESS consisting of three batteries is simulated with four groups of tuned filer parameters to verify the conclusion of balancing speed and power control accuracy. The parameters are shown in Table III.

The SOC balancing waveforms of the three batteries (#1–#3) are shown in Fig. 13. The initial SOCs of the batteries are 58%, 60%, and 62%, respectively. Thus, #1 is selected as ES, #2 as BC, and #3 as ED. The energy difference between ES and ED is about 17 280 J.

In the first group of simulation, the tuned filter resistance is set to 0.1 Ω. As shown in Fig. 13(a), with accurate tuned *LC*

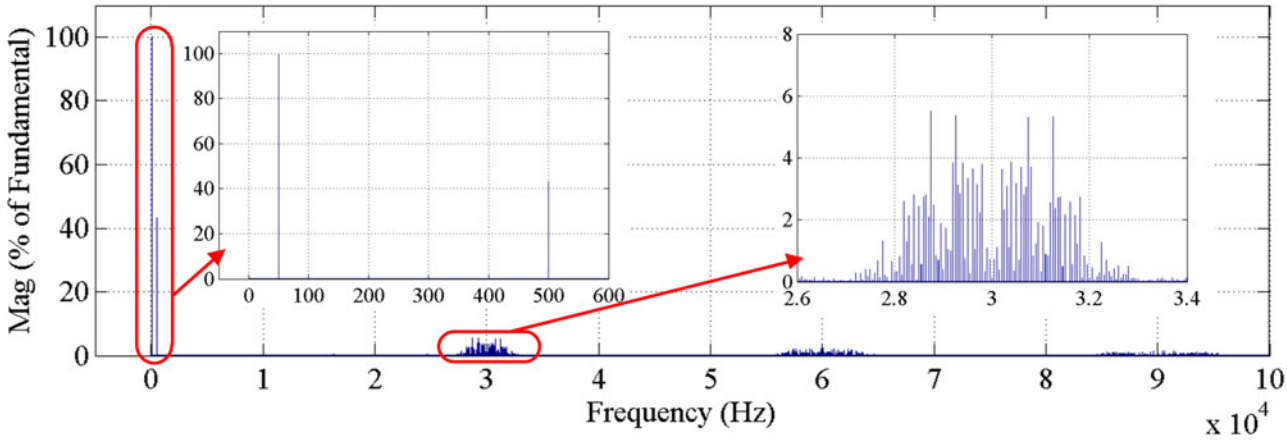

Fig. 11. FFT analysis of ν_s.

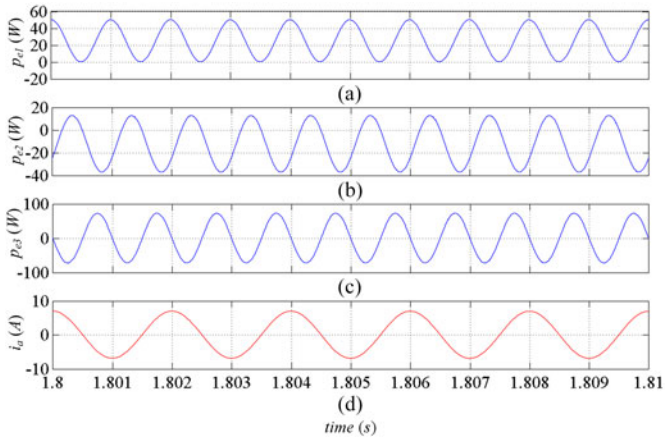

Fig. 12. Power exchange waveforms. (a) Exchange power of H-bridge 1. (b) Exchange power of H-bridge 2. (c) Exchange power of H-bridge 3. (d) Auxiliary current.

TABLE III
TUNED FILTER PARAMETERS

Symbol	Value
R_r	Group1: 0.1 Ω Group2–4: 0.2 Ω
C_r	Group1–4: 0.1013 mF
L_r	Group1–2: 1 mH Group3: 1.03 mH Group4: 1.1 mH
V_{c1}	Gourp1, 3, 4: 24 V Group 2: 25 V
V_{c2}	Group 1, 3, 4: 24 V Group 2: 23 V
V_{c3}	Group1–4: 24 V

values, the power exchanged can be controlled around 100 W and the SOC balancing process lasts about 160 s. Since the power exchange control is accurate, the BC only provides reactive power. It can be observed that decreasing speed of BC's SOC is constant. Meanwhile, the decreasing speed of ED is slower than that of ES before all SOCs are balanced because ED absorbs power from ES.

In the second group of simulation, the initial voltages of ES and ED are set at 25 and 23 V to verify the control strategy in dc voltage unbalance condition. Meanwhile, the tuned filter resistance increase to 0.2 Ω. As shown in Fig. 13(b), the SOC balancing time is doubled, but the power exchange relations are unchanged. Since the auxiliary modulation depth is adjusted according to the dc voltage of batteries, the SOC balancing is not affected by unbalanced dc voltage.

In the third group of simulation, the resonant inductance shifts 3% from the designed value. In Fig. 13(c), BC absorbs active power as revealed in (39). However, since the shift of the parameter is within designed tolerance, the SOC balancing speed is not affected. In Fig. 13(d), when resonant inductance shifts 10%, the SOC balancing control is no longer effective because the phase-shift angles in auxiliary loop are seriously destroyed. The simulation waveforms of SOC prove our analysis about exchanged power in auxiliary loop and the design of the tuned filter.

To prove the effectiveness of the proposed SOC balancing control in a multiple battery configuration, a BESS with nine batteries is built and simulated. The battery modules paralleled with the H-bridges are of different initial SOC values centered around 60%. As shown in Fig. 14(a), during the discharge simulation, the ESS provides active power to R_L. Meanwhile, the SOC values of battery modules are gradually balanced along with their respective discharge. During the SOC balancing process, the battery modules with maximum SOC transfers energy to the one with minimum SOC until all SOC values converge together. In Fig. 14(b), when the CMC does not provide active power to the load, the SOC balancing control is still effective. It is the main characteristic of the proposed topology to endow the auxiliary power loop with the ability to exchange power between energy storage components in standby mode, which grants the ESS with a large degree of control freedom.

The impacts of phase shift angle and the resonant inductance shift on power exchange and its efficiency are analyzed. First, the phase angles of ES and BC are set at $\varphi_1 = \frac{\pi}{2}$ and $\varphi_3 = \pi$. The phase angle of ED is set at $\varphi_3 = -\frac{\pi}{12}, -\frac{\pi}{6}, -\frac{\pi}{3}$, respectively. The power and efficiency waveforms are shown in Fig. 15(a) and (b). When $\varphi_3 = -\frac{\pi}{6}$, the auxiliary loop is at MPEP. The ED

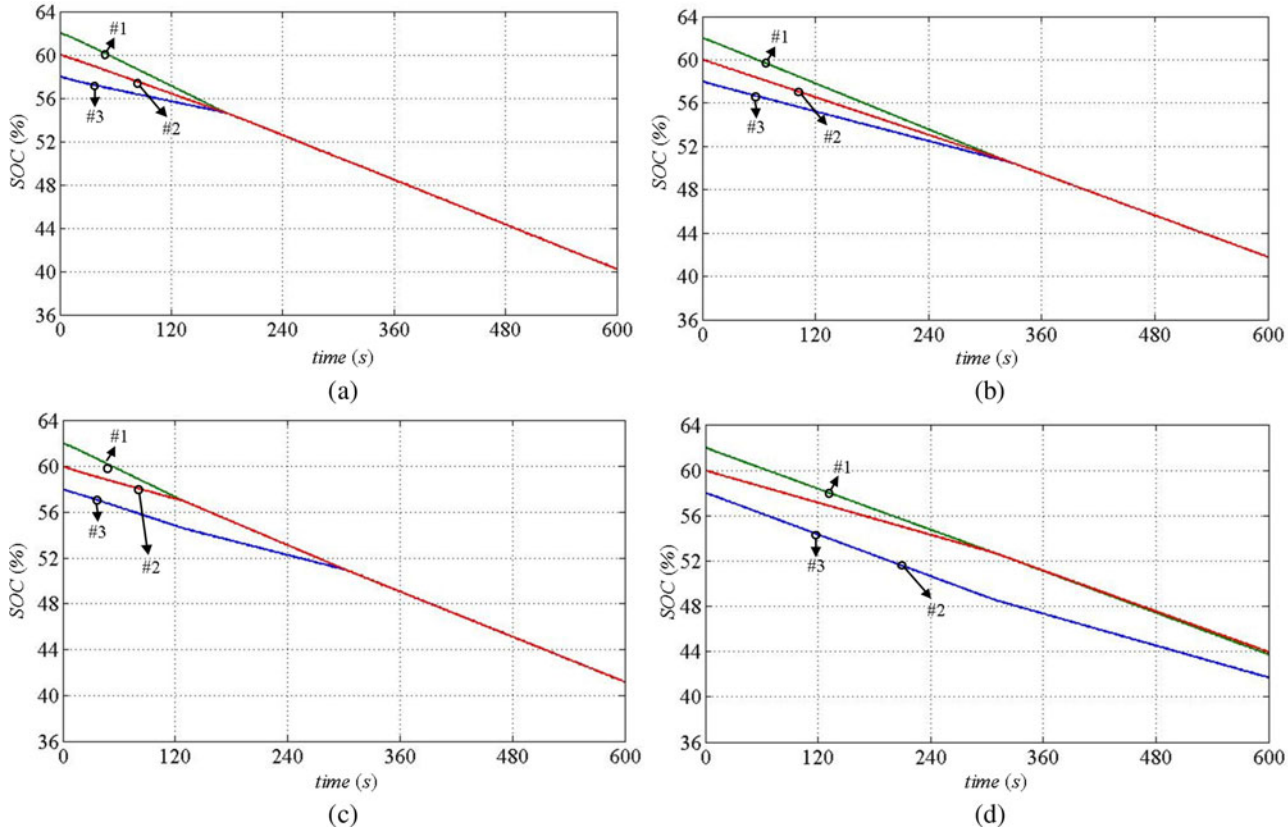

Fig. 13. SOC balancing control waveforms with different parameters. (a) Group 1. (b) Group 2. (c) Group 3. (d) Group 4.

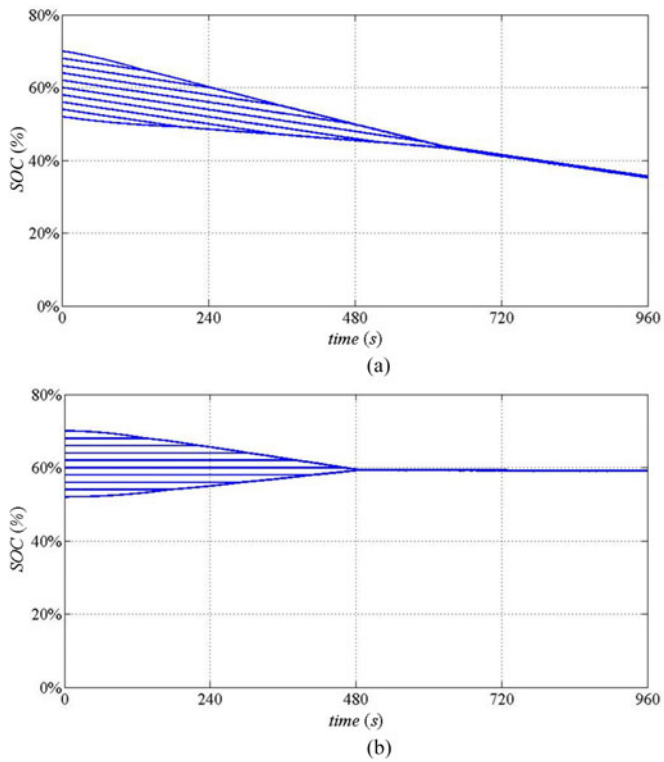

Fig. 14. SOC balancing control waveforms of nine batteries. (a) SOC balancing control during discharge. (b) SOC balancing control during standby.

absorbs maximum power and power exchange efficiency is 50%. When $\varphi_3 = -\frac{\pi}{12}$, the power provided by ES increases, while that absorbed by ED decreases. Thus, the efficiency decreases to 26%. When $\varphi_3 = -\frac{\pi}{3}$, the exchanged power and power loss both decreases, while the efficiency increases to 87.8%. The simulation result proves the analysis of the relation between power exchange and its efficiency as shown in Section II-C.

In another groups of simulation, the shift of L_r is set to -2%, -1%, 0%, 1%, and 2%. As shown in Fig. 15(c) and (d), the deviations of L_r effect on power exchange. When L_r is greater than its rated value, the power absorbed by ED decreases. That is because a certain percentage of the power ES provides is absorbed by BC in that condition. Conversely, when L_r is less than its rated value, BC transfers power to ED. Thus, the power exchange rated between ES and ED could exceed 50%. Meanwhile, the power loss is constant because the change of impedance of the tuned filter is very limited. These results prove the analysis of the resonant parameter shift in Section III-C.

To further verify the operation of the proposed topology and control methods, a 1-kW prototype BESS with three cascaded submodules was built, as shown in Fig. 16. The parameters are: $L_r = 2$ mH, $C_r = 50$ μF, $R_r = 2\ \Omega$, $L_f = 4.5$ mH, $C_f = 100$ μF, $R_f = 10\ \Omega$, $R_L = 200\ \Omega$, $V_c = 24$ μF, $f_m = 50$ Hz, $f_a = 500$ Hz, $f_c = 5000$ Hz. All switches are FF200R17KE3 MOSFET. The control strategy is implemented in TI TMS320F28335 digital signal processor (DSP). The DSP is responsible for collecting necessary measurements from the

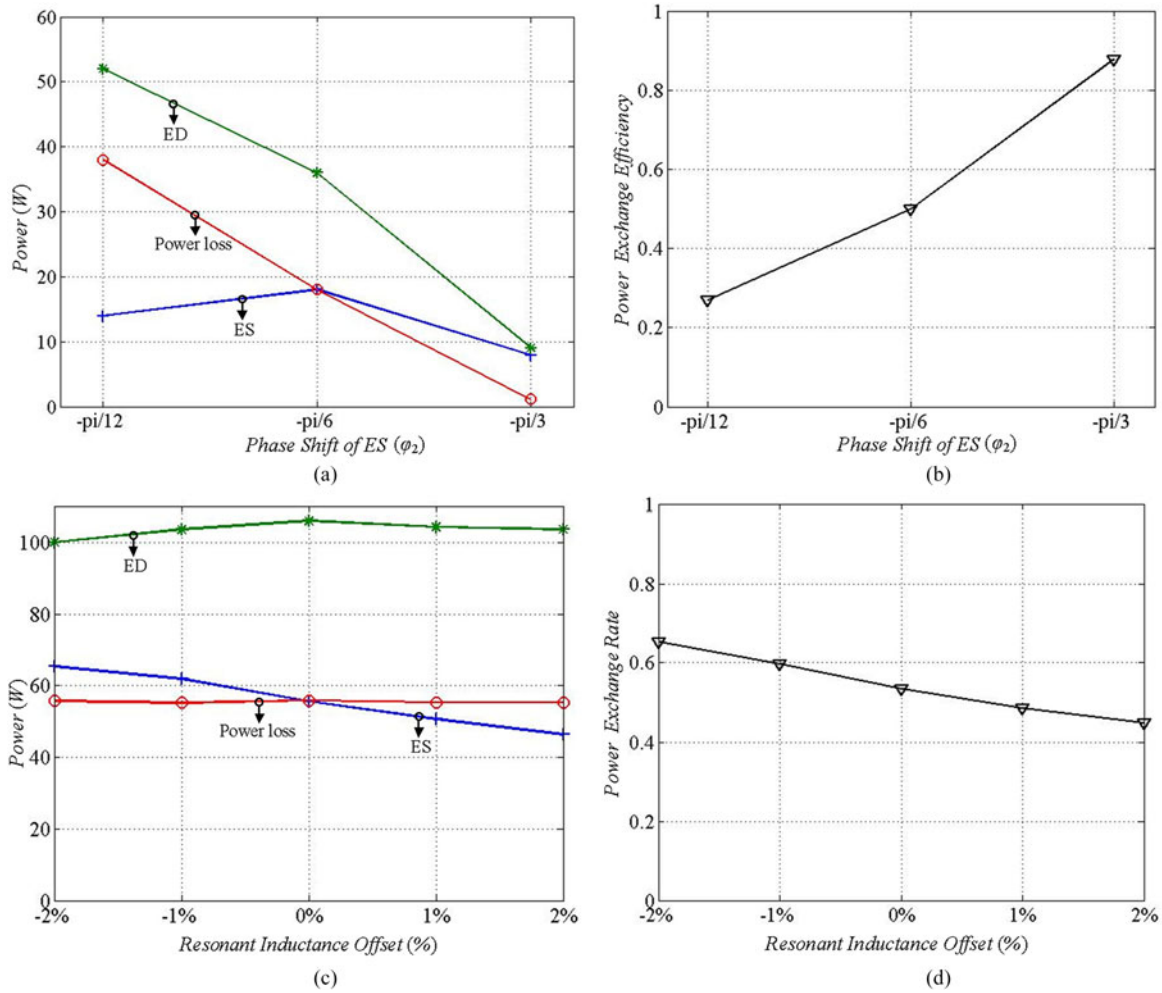

Fig. 15. Power and efficiency simulation. (a) Power with phase shift. (b) Power exchange efficiency with phase shift. (c) Power with resonant inductance shift. (d) Power exchange rate with resonant inductance shift.

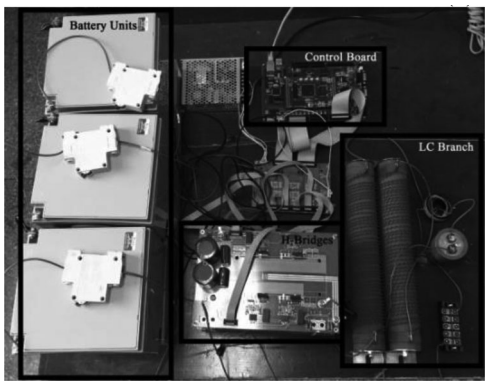

Fig. 16. 1 kW prototype with three H-bridges.

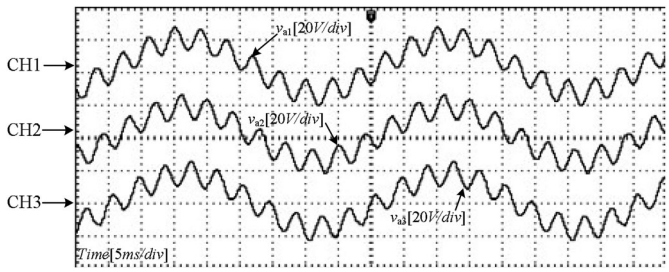

Fig. 17. Output voltage waveforms of three submodules.

system, i.e., the voltages/currents of the batteries and submodules. Based on these monitored data, the DSP calculates the modulation depths and duty cycles of the switches. The DF-PSC PWM signals are synthesized in VHDL-programmed CPLD module and distributed to MOSFET drive circuits. Meanwhile, the CPLD module is in charge of ensuring the protection from overvoltage and overcurrent in charging and discharging processes.

In the performance verification experiments, the fundamental and auxiliary modulation depths are set to 0.7 and 0.3, respectively. The phase differences of auxiliary frequency components between the three submodules are 120° and 90°. Fig. 17 illustrates the output voltages $\nu_{a1} - \nu_{a3}$ of the three submodules. To distinguish the fundamental and auxiliary components, the voltage waveforms are filtered by SINGLENT SDS1000CFL

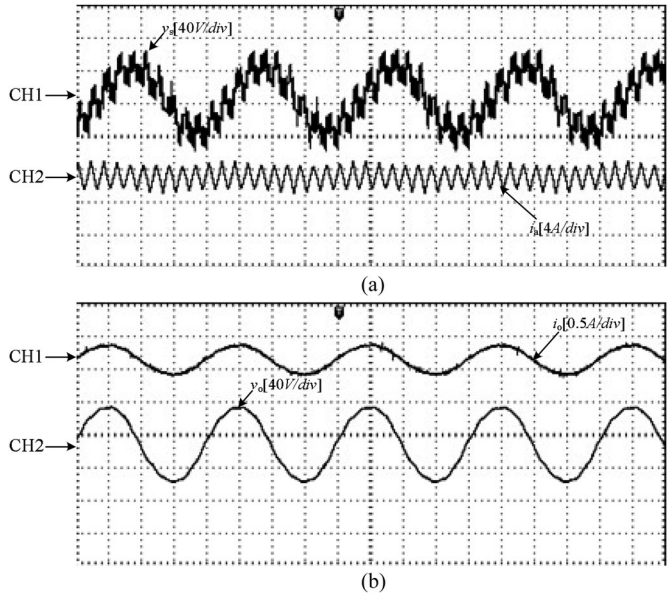

Fig. 18. Experimental result of the discharging procedure of the BESS. (a) ν_s and i_a. (b) ν_o and i_o.

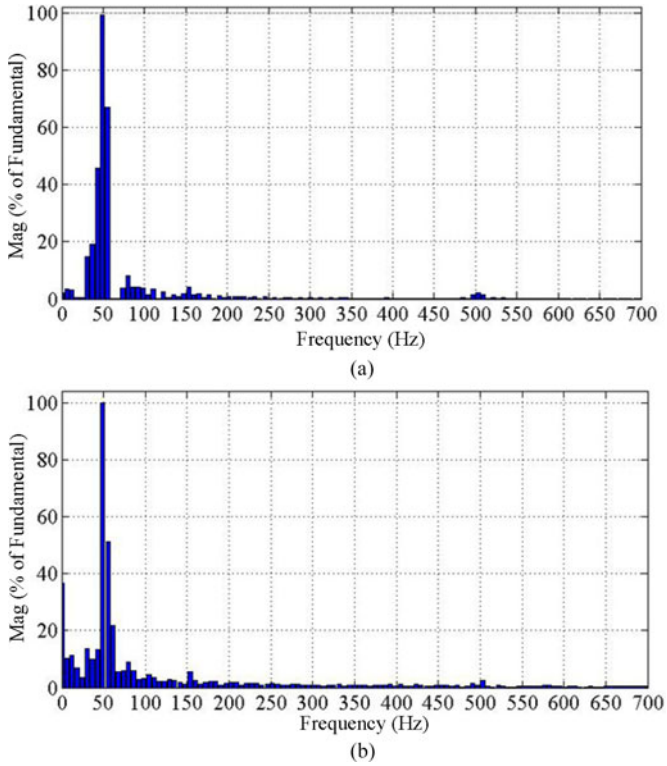

Fig. 19. FFT analysis result of the output voltage and current. (a) output voltage ν_o. (b) output current i_o.

oscilloscope. As shown in Fig. 17, the fundamental frequency components (50 Hz) are with the same phase. Meanwhile, the auxiliary frequency components (500 Hz) are with phase differences.

The voltage and current waveforms of BESS are shown in Fig. 18 to demonstrate the effectiveness of the filter design. In Fig. 18(a), the seven-level voltage waveform ν_s is obtained with DF-PSC PWM control, which contains both fundamental and auxiliary frequency components. i_a is the auxiliary loop current, which is obviously dominated by auxiliary frequency components. With the proposed resonant parameters design procedure, the fundamental frequency current has been filtered. Meanwhile, as shown in Fig. 18(b), the designed output filter eliminates the auxiliary frequency components in the output voltage. Thus, the output voltage ν_o and current i_o only contain 50-Hz sinusoidal component. The FFT analysis of ν_o and i_o in Fig. 19 demonstrated that the auxiliary frequency components (500 Hz) can be neglected. The 500-Hz alternating current i_a and 500 Hz voltage in $\nu_{a1} - \nu_{a3}$ produce the auxiliary power which is orthogonal to the output power. The power exchange between batteries is determined by the phase lags between i_a and high-frequency voltages.

The currents of three batteries during power exchange procedure are shown in Fig. 20. To make the 500-Hz component more obvious, the auxiliary modulation depth is raised to 0.7 in this group of experiment. The phase differences between the auxiliary frequency components of the three submodules are configured at the MPEP ($\varphi_1 = \frac{\pi}{2}$ and $\varphi_2 = -\frac{\pi}{6}$). Thus, the power exchange in the auxiliary power loop is maximized. CH1 and CH2 are the current waveforms of ES and ED, respectively. As shown in Fig. 20(a), the measured average current of cell1 is 2.38 A and of ED is –1.09 A. This phenomena proves that power is transferred from ES to ED via auxiliary

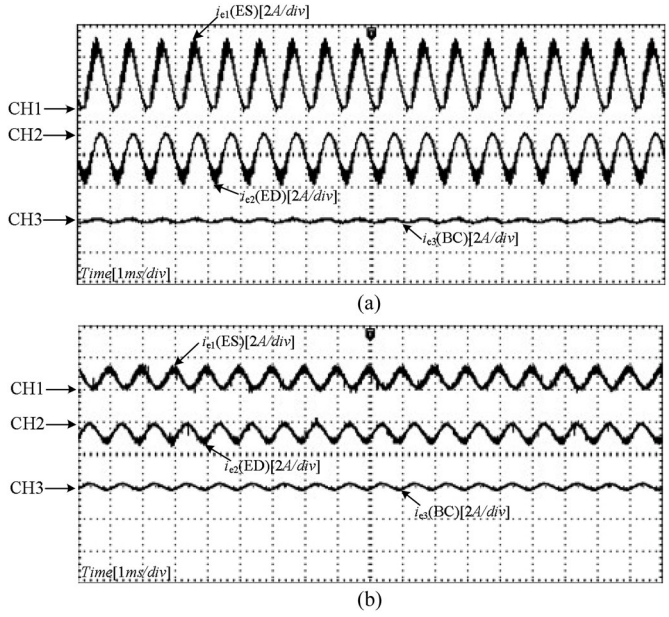

Fig. 20. Battery output current during power exchange procedure. (a) $\varphi_1 = \frac{\pi}{2}, \varphi_2 = -\frac{\pi}{6}, \varphi_3 = \pi$. (b) $\varphi_1 = \frac{\pi}{2}, \varphi_2 = -\frac{\pi}{4}, \varphi_3 = \pi$.

power loop. Since BC only provides reactive power, the average current of BC could be neglected. Based on (27), the maximum exchanged power between the two batteries is 35.28 W. The measured power absorbed by ED is 26.16 W. Considering other power losses like switching loss and reactive loss, the

experiment result could verify previous conclusion about power transfer with phase-shifted control. The exchanged power could be easily increased by reducing R_r in the auxiliary power loop. In Fig. 20(b), when $\varphi_2 = -\frac{\pi}{4}$, the positive discharge current of ES and negative charge current of ED both decrease. Consequently, the exchanged power between ES and ED will diminish. The experimental result of charge/discharge current of the batteries proves the effectiveness of DF-PSC PWM on power exchange control in CMC.

V. Conclusion

A novel CMC-based ESS, which contains an auxiliary power loop to exchange power between H-bridges, is proposed in this paper. The auxiliary power loop is realized by introducing a series *LC* branch into the CMC and applying the DF-PSC PWM. The mathematic analysis indicates that the voltages at fundamental frequency and auxiliary frequency are independent to each other with DF-PSC PWM. By controlling the phase differences between the auxiliary frequency voltages, power could be transferred from one H-bridge to another. However, we face a tradeoff between transferred power and efficiency. In CMC based BESS, the proposed power exchange mechanism could be used for SOC balancing. Simulation and experimental results verify the operation principle of the converter.

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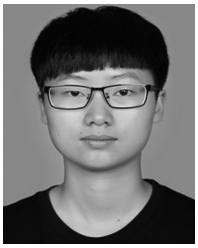

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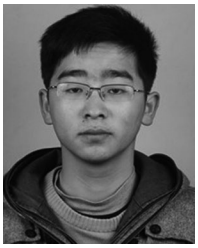

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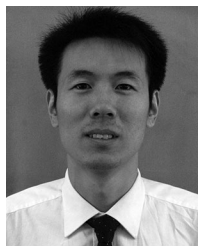

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